ABSTRACT OF THE DISCLOSURE

The burden of developing a complex bridge block imposed on the IP reuser is reduced by introducing a system clock into the IP. The IP composed of a functional circuit of this invention and its synchronizing circuit takes in the system clock by integrating the synchronizing circuit taking in the system clock with the IP functional circuit into the IP in reusing the IP complying with the standard in the development of an LSI with a built-in IP and its derivatives. This enables the reuser to incorporate the IP into the LSI via a simple bridge block, taking into account only the system clock for driving the system bus, which reduces the burden of handling the IP and increases the reusability of the IP.